Signal-Dependent Analog-to-Digital Converter Based on MINIMAX Sampling

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Abstract— **This paper presents a physical implementation of a signal-dependent analog-to-digital converter (ADC), called MINIMAX ADC. This ADC captures a sample every time an analog signal reaches its local maximum or minimum value. In this ADC, sampling naturally adapts to input signal frequency, which enables high data compression rate and power reduction to be achieved. A 8-bit MINIMAX ADC was implemented in 180nm CMOS technology. Measurement results show that the proposed MINIMAX ADC consumes lower power for less active signals, and the power reduction from conventional synchronous ADC is up to 20%.**

Keywords- signal-dependent sampling, MINIMAX, peak-detection, analog-to-digital converter

I. INTRODUCTION

Conventional synchronous analog-to-digital conversion and digital signal processing algorithms have been widely used in various applications. Traditionally, converters sample amplitude of analog signals consecutively with a constant time interval. In this approach, the sampling rate is determined by the maximal frequency in the signal spectrum. Therefore, for signals with high frequency components yet low activity, the conventional sampling is not power-efficient due to the high constant sampling rate.

For many applications with limited memory recourses and tight power consumption requirements, such as battery-powered sensing applications, alternative signal-dependent sampling schemes have been explored [1][2][3][4][5]. Use of non-uniform sampling provides various advantages for data acquisition, e.g. reduced number of samples (data compression), absence of aliasing, etc. However, it often suffers from difficulty of accurate signal reconstruction due to its high computational complexity [7].

A well-known signal-dependent sampling is level-crossing scheme [1]. Level-crossing ADC samples a signal when it crosses predefined threshold levels. As a result, non-uniformly spaced samples, whose local sampling density depends on the signal local properties, are obtained. This scheme requires at least two constantly operating comparators and two reference voltage circuits, which contributes to power consumption [2].

Another signal-dependent sampling approach, which is based on MINIMAX sampling, that captures a sample every time an analog signal reaches its local maximum or minimum value, is proposed in [6]. The voltage amplitude of the sample is quantized and the time elapsed after the previous sample is measured by a local timer. MINIMAX sampling naturally adjusts sampling frequency depending on input signal frequency. In fact, [6] reported that MINIMAX sampling scheme provides relatively high data compression rate and high reconstruction precision compared to level-crossing scheme, while no physical implementation was presented.

Reference [13], which is the preliminary work of this paper, proposed a power-efficient and signal reconstruction-friendly architecture of MINIMAX ADC consisting of a peak detector, a timer and an amplitude quantizer circuit. Power consumption is reduced by storing an analog signal at discrete time intervals with a sample-and-hold circuit and performing AD conversion for the stored signal only when a signal peak is detected. Such non-uniform yet discretely sampled signal is highly compatible with traditional signal processing algorithms since peak samples are inherently located on a uniform grid and only missing samples on the grid need to be reconstructed.

This paper details the implementation of MINIMAX ADC and presents measurement results of the prototype chip fabricated in 180nm CMOS technology. Measurement results show that the MINIMAX ADC consumes lower power for less active signals, and the maximum power reduction is 20%.

The remainder of this paper is organized as follows: Section II explains MINIMAX sampling and presents the proposed architecture of MINIMAX ADC. Section III describes the physical implementation of MINIMAX ADC. Measurement results are presented in Section IV. Section V concludes the discussion.

II. MINIMAX ADC

A. *MINIMAX Sampling*

Fig. 1 illustrates an example of MINIMAX sampling, which was proposed in [6], where one sample is captured for each peak of an analog signal. One of the advantages of MINIMAX sampling is the ability to reconstruct an analog signal from reduced number of samples. Reference [6] reported that it is theoretically possible to reconstruct an analog signal from MINIMAX samples with relatively high precision if the exact timings of the peaks are known. However, the signal reconstruction from non-uniform peak samples is

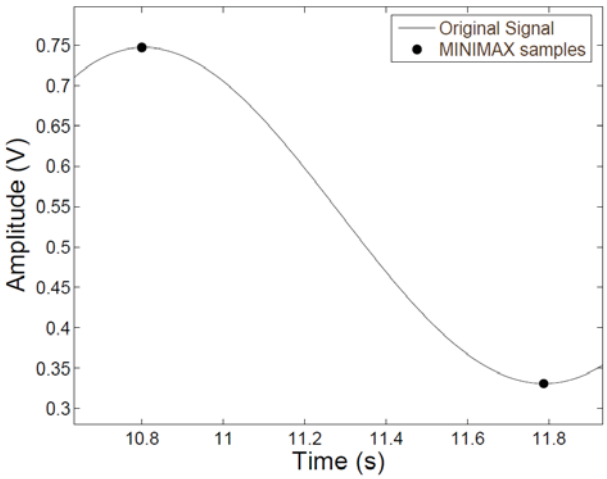

Figure 1: MINIMAX Sampling.

computationally expensive, and [6] presented an iterative reconstruction algorithm.

In [13], we proposed an implementation where the signal reconstruction becomes more straightforward and no iterative reconstruction algorithms are necessary. This becomes possible because samples generated by the proposed MINIMAX ADC are non-uniform yet located on a uniform grid. Missing samples on the grid are reconstructed by using piecewise cubic Hermite interpolation (PCHIP). This interpolation method does not induce excessive variation between data points and provides good reconstruction results processing MINIMAX samples, compared to, such as, polynomial interpolation [14]. Using this approach, signal reconstruction error is reasonably low if the timer frequency, which defines the grid, is 10 times higher than analog signal frequency.

B. MINIMAX ADC Architecture

Fig. 2 shows the architecture of the proposed ADC for MINIMAX sampling composed of a peak detector, a discrete timer and an amplitude quantizer circuit. The peak detector finds peaks of a given analog input voltage V_{ANALOG}, and gives triggers *trig* to the amplitude quantizer circuit and timer.

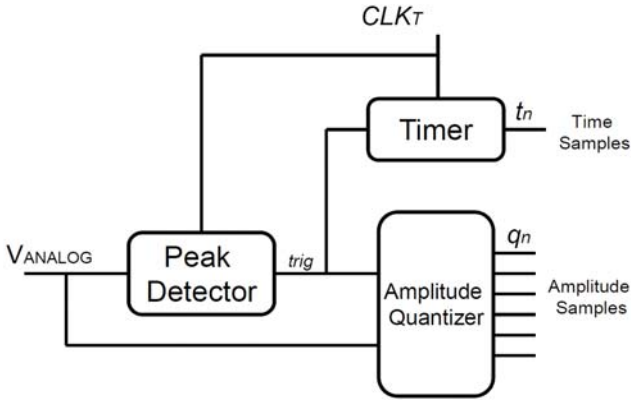

Figure 2: Structure of MINIMAX ADC.

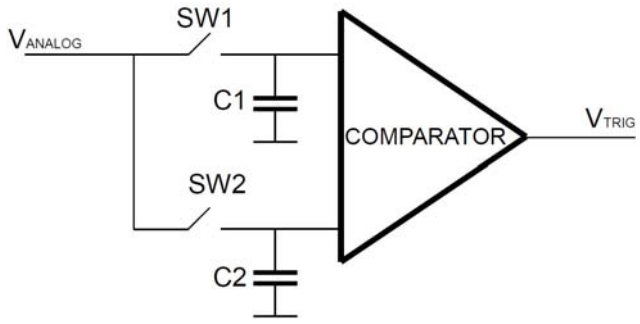

Figure 3: Switched-capacitor Peak Detector.

Conventional synchronous ADC can be used as an amplitude quantizer. This amplitude quantizer works only when peaks are detected. For minimizing power dissipation, low-power synchronous ADC should be selected as the amplitude quantizer. For that purpose, Successive Approximation Register (SAR) ADC [9] is suitable.

The key circuit of MINIMAX ADC is the peak detector, which enables signal-dependent sampling. The peak detector and timer are driven by a timer clock CLK_T, which attains higher compatibility with traditional signal processing algorithms, since all samples are located on the grid of CLK_T. An implementation of peak detector is shown in Fig.3. It consists of a comparator, two capacitors and two switches. These pairs of capacitor and switch work as sample-and-hold circuits which are used for storing previous and current amplitude values of V_{ANALOG} for comparison. In this configuration, when a peak occurs, the comparator generates a transition, which enables peak detection and triggers the timer to count the time between two adjacent peaks.

Fig. 4 exemplifies 3-bit amplitude quantizer using SAR ADC based on charge-redistribution DAC [9], and Fig. 5 presents its timing diagram. Assuming that a sample of analog signal S0 was previously sampled, the next sample S1 will be sampled to capacitor C1 of the peak detector through switch SW1 (Fig.2) and also to capacitor array C_{MSB1} of the SAR ADC through SW3 (Fig.4). The following sample S2 will be sampled to C2 through SW2 and also to C_{MSB2} through SW4. When the difference between two adjacent samples changes its sign, the comparator will generate V_{TRIG} signal. After that, switch SW5 is turned on, which will trigger the charge-redistributional conversion of sample S1 using simple digital inverters. Finally, the digitally represented voltage of sample S1 will appear on the output of SAR logic after the conversion finishes.

III. IMPLEMENTATION

The proposed architecture of 8-bit MINIMAX ADC was implemented in 180nm CMOS technology with 1.8V supply voltage.

The value of sample-and-hold capacitors (C1 and C2) shown on Fig.3 is 2pF. The switches are implemented as

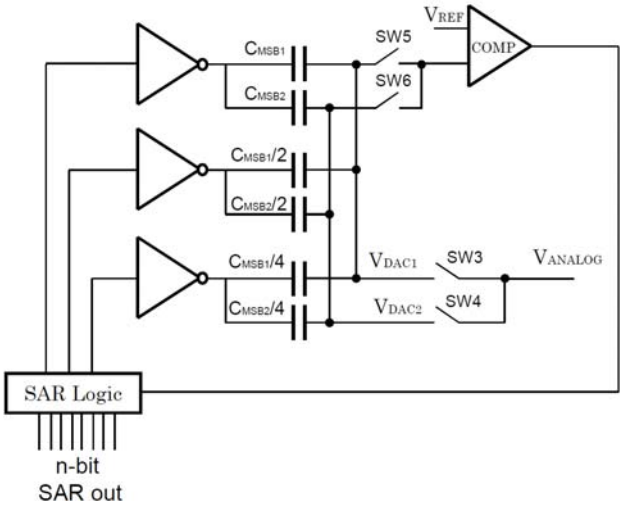

Figure 4: Amplitude Quantizer using SAR ADC.

PMOS and NMOS transistors connected in parallel and driven by logic.

To reduce DC power that is often dissipated by analog bias current, clocked comparator [2][9][10][15] is desirable and used in this work. The 8-bit SAR ADC, which is an extension of Fig. 4, consists of a comparator, binary-weighted capacitor array and digital inverters, controlled by SAR logic [9]. Two arrays of C_{MSB} ($C_{MSB}=C_{MSB1}=C_{MSB2}$) capacitors were implemented to store two consecutive samples. One of those two samples will be converted after the peak detection. The value of C_{MSB1} and C_{MSB2} is 12.8pF. The capacitor arrays were implemented as MIM capacitors.

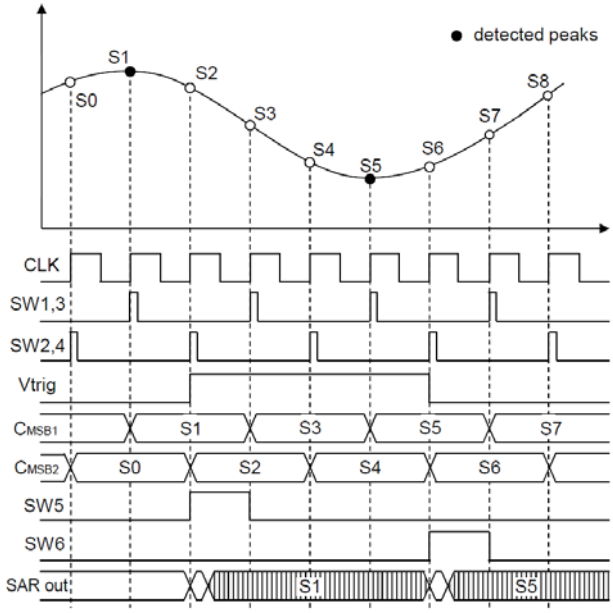

Figure 5: Timing Diagram of MINIMAX ADC.

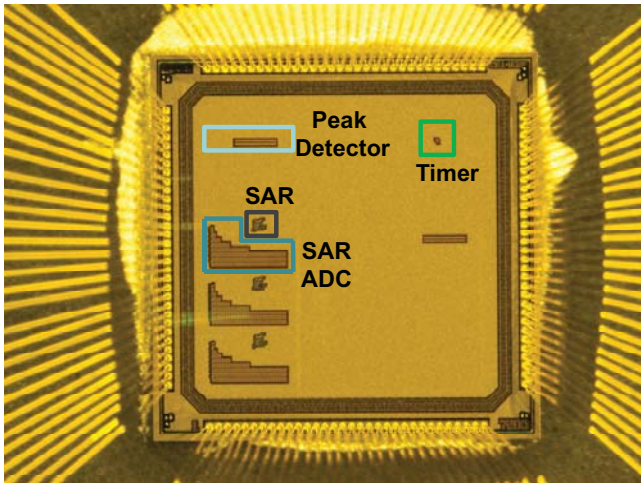

Figure 6: Micrograph of the Prototype Chip.

Let us briefly explain the operation of SAR ADC. Suppose the left side of capacitors is switched from low to high. In this case, VDAC increases by $\Delta V_{DAC}=VDD*C_{MSB}/C_{TOTAL}$, where C_{TOTAL} is the total capacitance of the DAC output node and VDD is the supply voltage of inverters. Conversely, when the left side of C_{MSB} is switched from high to low, the output returns to its original value. First, the DAC is reset to a state when the MSB is high and all other bits are low. Next, V_{ANALOG} is sampled into C_{MSB} and then compared to V_{REF}. The comparator makes a decision if the MSB should remain high or set to low. Next, the MSB-1 is set to high and the procedure is repeated until N comparisons have been done for N bits. The comparison for 8 bits will finish after all 8 inverters are consecutively triggered. Finally, the SAR logic will have a digital representation of the analog voltage.

IV. Measurement Results

The designed chip was fabricated in 180nm CMOS technology. The supply voltage is 1.8V. The micrograph of the chip is shown in Fig. 6. The die size is 2.5mm x 2.5mm. The area of the MINIMAX ADC is approximately 0.23mm^2. The MIM capacitors for switched peak detector and SAR ADC consume 80 % of the total area.

Saw wave signal whose peak-to-peak amplitude was 1.6V was given to the MINIMAX ADC as a signal example. The timer frequency was set to 10 kHz.

Since the proposed ADC is targeted for low power applications it has been assumed that signal reconstruction will not be done on the same chip. Therefore, power overhead of reconstruction filter is not discussed here.

Fig. 7 shows the measured power dissipation of MINIMAX ADC with a switched capacitor peak detector, and demonstrates that its power consumption depends on the activity of input signal. The power dissipation of the synchronous SAR ADC is also shown in Fig. 7. Here, ratio of peaks is defined as the number of peaks divided by the number of points on the timer grid. At ratio of peaks = 0%, analog input signal is constant, while at ratio of peaks = 100% the AD conversion is done at every timer period. The ratio was varied

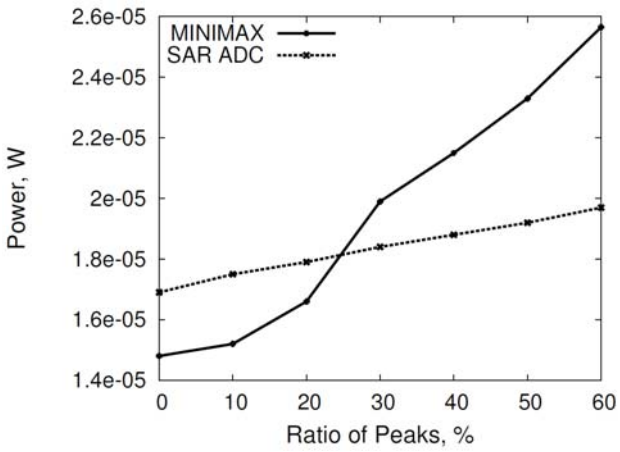

Figure 7: Measured Power Consumption of MINIMAX ADC.

by changing the number of peaks per the observation period.

In synchronous SAR ADC, AD conversion is carried out continuously. Therefore, ideally, the power consumption should be roughly constant. Practically, there is a slight increase of the power consumption for signal with higher activity. When input signal is inactive, SAR ADC will not be operating since the peak detector does not generate trigger signal, and, therefore, the power consumption of SAR ADC in MINIMAX ADC becomes quite low. In fact, when the ratio is lower than 25%, the proposed ADC attains lower power operation. In speech and also various biomedical signals, e.g. neural spikes with low occurrence rate, value of ratio of peaks is often much smaller than 20% [16] and, therefore, the proposed ADC is more efficient than conventional synchronous ADC. For example, at 20% ratio of peaks the power reduction is 9%, and at 10% ratio of peaks the power reduction is 18%. The maximal power reduction of this implementation is 20%.

In the current implementation of the peak detector, the peak detection threshold, which is defined as voltage amplitude difference in successive timer timings necessary for peak detection, is 100mV. At lower threshold values, even small variations of analog signal can be detected, but it will increase the number of acquired samples. On the other hand, higher threshold values compress the digitized data. Thus, depending on the application and required reconstruction accuracy, the peak detection threshold needs to be carefully determined.

The maximum conversion rate of MINIMAX ADC is approximately 1.25MS/sec, which is mainly limited by delay of internal DAC in the conversion circuitry.

V. Conclusions

This paper demonstrated that MINIMAX ADC can be effective for signals with low or changing activity. This sampling naturally adapts to input signal frequency and allows saving power dissipation during inactive periods of input. The structure of MINIMAX ADC with switched-capacitor peak detector circuit was implemented in 180nm CMOS technology.

The measurement results confirmed that power reduction can be obtained for input signals whose peak ratio is lower than 25%. At 20% ratio of peaks the power reduction is 9%, and at 10% ratio the power reduction is 18%. The maximal power reduction of this implementation is 20%. In addition to power reduction, an analog signal can be reconstructed after MINIMAX sampling from reduced number of samples.

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