Background

- The spread of LCD
  - Demand high resolution
- Deinterlace
  - Conversion from interlaced video to progressive video
  - Implemented in LCD TVs
    - real-time processing on hardware
  - Various methods exist
    - MC method is most popular

A novel hardware architecture for deinterlacing is proposed

- Reduces hardware cost keeping the quality of deinterlaced video sequence high.
  - The propose architecture is based on an Inpainting-based deinterlacing method[1]

Inpainting-based deinterlacing method[1]

- Interpolate the line by selected bipixels

Node: expresses a bipixel, which is a pair of two pixels (candidate pair for interpolation).
Weight: Cost for interpolation of the current bipixel.

(0,1): bipixel, which is composed of pixels $x^- = 0$ and $x^+ = 1$.

Route is limited by directional edge

Bipixels are selected by searching shortest-paths

- Use spatial interpolation and temporal interpolation

To realize real-time processing

- The time for processing deinterlace of a line
  - **The time limit** (Full HD 1080p60)
    - ≈ about 3,900 cycles@124MHz (time to output 2 lines)

A data hazard:
- reading result of searching shortest-paths

⇒ Implement the architecture which reduces the number of cycles for searching shortest-paths to realize real-time processing

Horizontal resolution: $W$
The proposed architecture is designed using Verilog-HDL, and synthesized using 0.13μm CMOS technology. $W = 1920$ (in Full HD input)

<table>
<thead>
<tr>
<th>Gate count @133MHz</th>
<th>Max frequency</th>
<th>SRAM</th>
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<tbody>
<tr>
<td>942,998</td>
<td>199 MHz</td>
<td>390 Kbit</td>
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The time processing for a line on Proposed architecture:

About 4000 cycles@166MHz

The time limit for real-time processing:

About 3900 cycles@124MHz = about 5000 cycles@166MHz