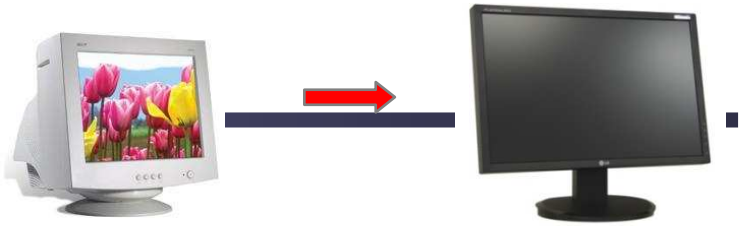
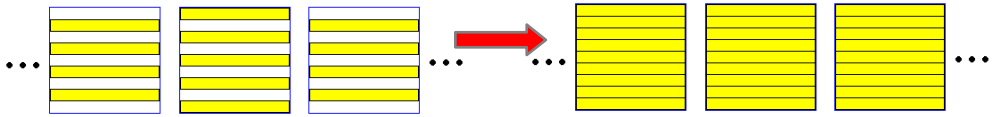
Background





- The spread of LCD
  - Demand high resolution
- Deinterlace
  - Conversion from interlaced video to progressive video
  - Implemented in LCD TVs

⇒ **real-time processing on hardware**

  - Various methods exist

⇒ **MC method is most popular**

Motion compensated deinterlacing

- High quality, but
- Requires high computational cost

⇒High cost on hardware

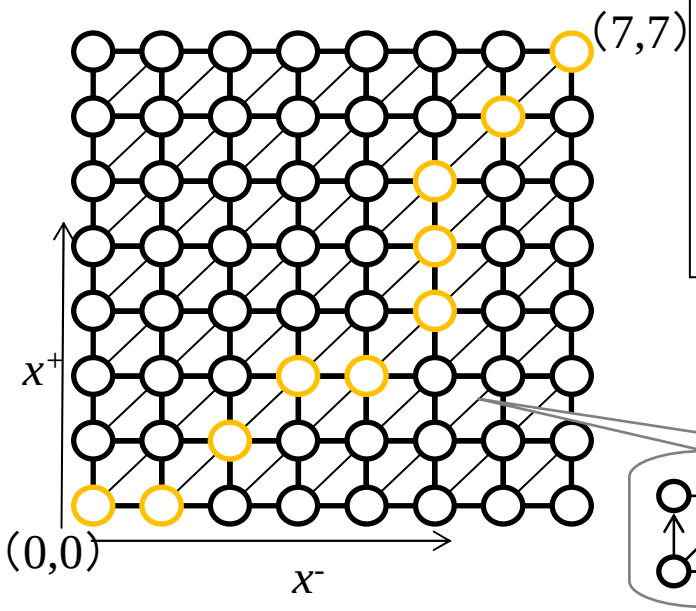
A novel hardware architecture for deinterlacing is proposed

- Reduces hardware cost keeping the quality of deinterlaced video sequence high.
  - The propose architecture is based on an Inpainting-based deinterlacing method[1]

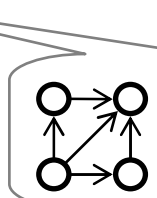
[1] C. Ballester et al., “An Inpainting- Based Deinterlacing Method,” IEEE Trans. IP, Vol. 16, No. 10, Oct. 2007.

Inpainting-based deinterlacing method[1]

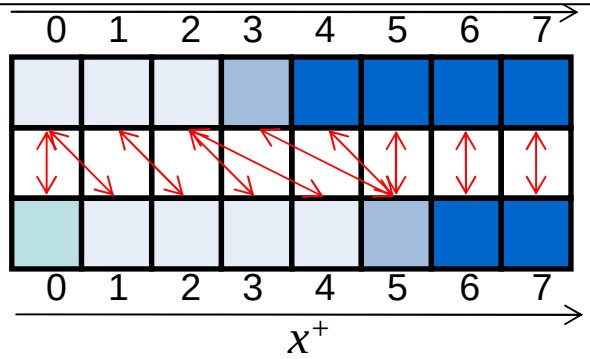
- Interpolate the line by selected bipixels



Node: expresses a bipixel, which is a pair of two pixels (candidate pair for interpolation).
Weight: Cost for interpolation of the current bipixel.
(0,1): bipixel, which is composed of pixels x^- = 0 and x^+ = 1.

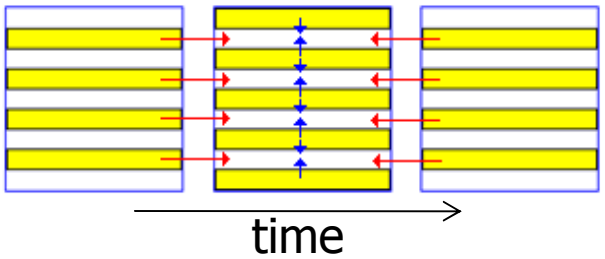


Route is limited by directional edge



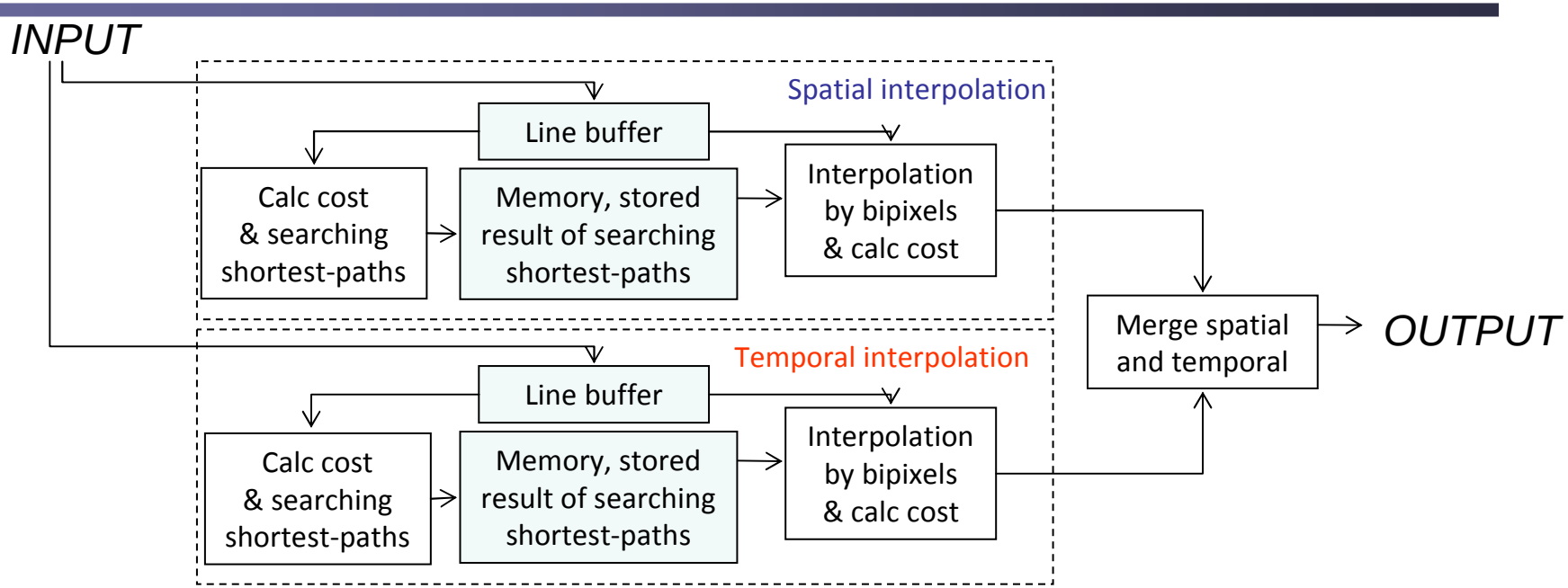
Bipixels are selected by searching shortest-paths

- Use spatial interpolation and temporal interpolation



[1] C. Ballester et al., “An Inpainting- Based Deinterlacing Method,” IEEE Trans. IP, Vol. 16, No. 10, Oct. 2007.

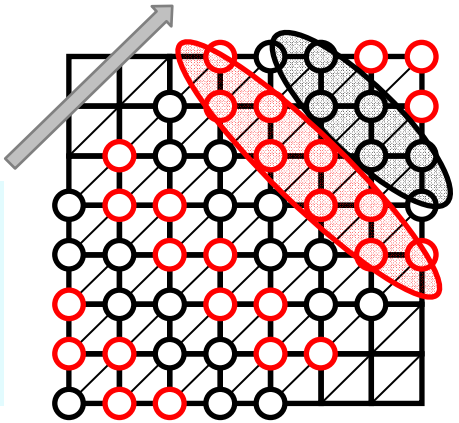
Proposed Architecture



- To realize real-time processing
  - The time for processing deinterlace of a line

The time limit (Full HD 1080p60)
＝about 3,900 cycles@124MHz (time to output 2 lines)

Horizontal resolution : W



A data hazard :
reading result of searching shortest-paths
⇒Implement the architecture which reduces the number of cycles for searching shortest-paths to realize real-time processing

Implementation result

- The proposed architecture is designed using Verilog-HDL, and synthesized using 0.13μm CMOS technology.
  - W = 1920（in Full HD input）

Gate count @133MHz	Max frequency	SRAM
942,998	199 MHz	390 Kbit

The time processing for a line on Proposed architecture

About 4000 cycles@166MHz

<

The time limit for real-time processing

About 3900 cycles@124MHz
＝about 5000 cycles@166MHz