"RF Channel Filtering: a Revival of N-Path Filters in Nanometer CMOS?"

Bram Nauta
University of Twente, The Netherlands

Abstract: In the 1960’s research was carried out on so called N-path filters. These filters exploited down conversion filtering and again up conversion. This way band-pass filters could be made from low-pass filters. The techniques lost attention because the matching of capacitors turned out to be a problem and soon “real” oversampled Switched Capacitor filters took over attention, which have become classical. However in modern nanometer CMOS the capacitor matching is almost perfect and the speed of up the down and up-converters is in the GHz range which makes it worth to have a look at these techniques and to improve the architectures. Moreover with today's speed of digital circuits the required multiphase clock signals can be easily generated for RF frequencies. The result is a filter which shows more or less analog behavior while just using switches, digital gates and capacitors. After discussing the basics of N-path filters a fourth-order bandpass filter and a second order notch filter, both tunable over a decade in frequency, will be discussed.

Speaker Biography: Bram Nauta was born in Hengelo, The Netherlands. He received the M.Sc and PhD degree from the University of Twente, Enschede, The Netherlands in 1987 and 1991 respectively. After that he joined Philips Research, Eindhoven the Netherlands and 1998 he returned to the University of Twente, as full professor heading the IC Design group.

He was the Editor in Chief of IEEE Journal of Solid-State Circuits (2007-2010) and is the Chairman of the technical program committee of the 2013 International Solid State Circuits Conference (ISSCC). He is also member of the programme committee of ESSCIRC and VLSI symposium. He is co-recipient of the ISSCC 2002 and 2009 "Van Vessem Outstanding Paper Award", is distinguished lecturer of the IEEE, elected member of IEEE-SSCS AdCom and is IEEE fellow.
"Time-Domain Analog and RF Signal Processing"
Robert Bogdan Staszewski
Delft University of Technology, The Netherlands

Abstract: One of the most important developments in the wireless industry within the last decade was the invention and popularization of the time-domain analog/RF microelectronics. The new paradigm revolves around a bold premise of “the superiority of a time-domain operation over the traditional voltage-domain operation” in which the time-stamps, rather than the voltage or current levels, are the information carrier. This approach works surprisingly well in nanoscale CMOS processes, being nowadays the mainstream process technology for consumer electronics, with their rising and falling transition times on the order of 10 picoseconds as well as extremely low energy consumption due to the fact that only 100 or so electrons are involved in each transition. This new paradigm has been successfully exploited by this author while at Texas Instruments in Dallas, Texas, USA, to transform the entire wireless transmitter/receiver architecture in which the analog and RF circuits operate now in the time-domain. Specifically, a time-to-digital converter (TDC) and a digitally-controlled oscillator (DCO), which form an all-digital phase-locked loop (ADPLL), have been proposed to significantly improve the frequency synthesizers operating at multi-GHz frequencies. New infinite-impulse response (IIR) filters have been proposed to process weak antenna signals in the new discrete-time receiver architecture. This new approach drastically improves cost, area/volume, energy consumption and integration level of analog electronic circuits. Consequently, the majority of the 1.6 billion cell phones produced annually are now based on this approach. However, this author believes that the time-domain analog revolution has merely begun and the best is yet to come with new aspects (e.g., ultra-low power, millimeter-wave), circuits (e.g., ADC, DAC) and applications (e.g., satellite communications; non-wireless, such as 3D imagers) begging to be exploited. This talk revisits this exciting journey and offers glimpse of future developments.

Speaker Biography: R. Bogdan Staszewski received BSEE (summa cum laude), MSEE and PhD from University of Texas at Dallas, USA, in 1991, 1992 and 2002, respectively. From 1991 to 1995 he was with Alcatel in Richardson, Texas. He joined Texas Instruments in Dallas, Texas in 1995. In 1999 he co-started a Digital RF Processor (DRPTM) group with a mission to invent digitally-intensive approaches to traditional RF functions. Dr. Staszewski has served as a CTO of the DRP group between 2007 and 2009. Since July 2009 he is Associate Professor at Delft University of Technology in the Netherlands. He has co-authored one book, four book chapters, 135 journal and conference publications, and holds 100 issued and 50 pending US patents. His research interests include nanoscale CMOS architectures and circuits for frequency synthesizers, transmitters and receivers. He is an IEEE Fellow.
"Advanced Digital RF MIMO Transceiver for Next Generation Mobile Communication"

Hyun-Kyu Yu
Electronics & Telecommunications Research Institute, Korea

Abstract: The RF front-end is the last exempt and barrier to be true digital convergence on the hand-held phone. Some pioneers dream SDR ideally or try practical digital intensive transceiver such as DRP of TI. A new Digital RF Transceiver SoC with minimum analog signal processing is introduced. The receiver is composed of only three blocks: LNA, Direct Digital Converter (DDC), and external SAW. In the transmitter, the digital baseband signal is directly converted to the RF by Direct RF Converter (DRFC). Most analog signal processing is done at the Digital Front End (DFE). This novel architecture was applied successfully to the 3G LTE transceiver at the band of 2.1GHz with variable bandwidth of 1.4/3/5/10/15/20MHz. The design details and implementation results will be presented on the spot.

Speaker Biography: Hyun-Kyu Yu received the B.S. and M.S. degrees in electronics engineering from Kyungpook Nat’l University in 1981 and 1983 respectively, and the Ph.D. degree in electrical and electronics engineering from KAIST in 1994. In 1983, he joined the ETRI, where he worked on both devices and circuit technologies on CMOS, VDMOS, PSA BJT, 4M/16M/64M DRAM, SOI MOSFET modeling, and standard cell library. Since 1996, he has led RF/Analog IC design team that successfully developed the world first CMOS based Rx/Tx chips for the CDMA and PCS cellular phone in 1999 and 2001 respectively. He also directed several tasks in the area of RFIC including digital TV tuner, DDFS, IEEE 802.11.a/b, WCDMA handset, Digital Multimedia Broadcasting, and 10Gbps SerDes. Since 2006, he has been the director of RF Circuit Group which includes research on mm-wave applications such as 60GHz WPAN and 77GHz/94GHz radar sensor system in SiGe and/or compound semiconductor devices including HEMT and HBT. More recently, he worked on Digital RF transceiver SoC for mobile TV and 3G LTE application. And he is currently responsible for SW-SoC Convergence Laboratory as a senior vice president of ETRI.

Dr. Yu is a board member of IEEK and a senior member of IEEE. He founded and has been serving as chairman of the RF Integrated Circuit Technology Society in Korea since 2000. He has received several awards including Nat’l Award from Government for the contribution to the research on RF CMOS technologies. He is the author and co-author of over 120 technical papers and 100 patents in the RF devices, circuits, and system design areas.
"Sensor Enabled UHF Passive RFID Tag for Wireless Monitoring Applications"
Man-Kay Law
University of Macau, China

Abstract: Passive RFID tags operating in the UHF band compliant to EPC Gen-2 have been widely adopted in various applications. Combined with embedding sensory systems, various wireless monitoring applications can be readily accomplished. The challenge, however, is the realization of ultra-low power sensing with system level optimization to alleviate the potential degradation in the tag operating distance.

We will present a system-on-chip passive RFID tag with an embedded temperature sensor for the EPC Gen-2 protocol in the 900-MHz UHF band. With system level optimization and co-designing of system building blocks, temperature sensing using nanowatt additional power consumption can be accomplished. Fabricated in a standard 0.18-µm CMOS process, the 1.1-mm² tag chip is bonded onto an antenna using flip-chip technology to realize a complete tag inlay, which is successfully demonstrated and evaluated in real-time wireless communications with commercial RFID readers. The tag inlay achieves a sensitivity of -6 dBm and a sensing inaccuracy of ±0.8°C (3σ) over operating temperature range from -20°C to 30°C with one-point calibration.

Speaker Biography: Man-Kay Law received the B.Sc. in Computer Engineering and the PhD degree in Electronic and Computer Engineering from Hong Kong University of Science and Technology (HKUST), in 2006 and 2011, respectively. From February 2011, he joined HKUST as a Visiting Assistant Professor. He is currently an Assistant Professor in the State Key Laboratory of Analog and Mixed-Signal VLSI, Faculty of Science and Technology, University of Macau. His research interests are in the area of ultra-low power energy harvesting and sensing circuits for wireless sensing and biomedical systems, with special emphasis on smart CMOS temperature sensors, CMOS image sensors, ultra-low power analog design techniques, and integrated energy harvesting techniques. He currently serves as a member of the IEEE Circuits and Systems Society (CASS) technical committee on Sensory Systems as well as Biomedical Circuits and Systems.
"Low Power Circuits for Body Area Network (BAN)"

Jerald Yoo

Masdar Institute of Science and Technology, United Arab Emirates

Abstract: We are facing a new era of semiconductor, from technology-driven towards application-driven evolution. Currently, chronic diseases account for over 1/3 of deaths around the world, and to deal with this, healthcare paradigm is shifting from reactive illness management towards proactive and preemptive health management; the goal here is to maintain healthy life in the first place, or prevent illness from getting any worse by continuously monitoring health during normal daily life.

Body Area Network (BAN) is a strong candidate to realize continuous health monitoring environment. A popular approach to form a BAN is by adopting RF radio communication; however, interference and security issues limit the RF approach to be the ultimate solution. Wearable BAN can complement the RF by using a conductive channel on fabric or a body channel, and this gives the circuit society a chance to lead another evolution.

Speaker Biography: Jerald Yoo received the B.S., M.S., and Ph.D. degrees in Department of Electrical Engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2002, 2007, and 2010, respectively.

In May 2010, he joined the faculty of Microsystems Engineering, Masdar Institute of Science and Technology, Abu Dhabi, United Arab Emirates, where he is an assistant professor. During June 2010 to June 2011, he was also with Microsystems Technology Laboratory, Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, as a visiting scholar. He developed low-energy Body Area Network (BAN) transceivers and wearable body sensor network using Planar-Fashionable Circuit Board (P-FCB) for continuous health monitoring system. His research focuses on low energy circuit technology for wearable bio signal sensors, wireless power transmission, SoC design to system realization for wearable healthcare applications, and energy-efficient biomedical circuits. He is an author of the book chapter in Biomedical CMOS ICs (Springer, 2010).

"Low-power RFIC design for 60GHz system-on-chip applications"

Kaixue MA (Speaker) and Kiat Seng YEO
Nanyang Technological University, Singapore

Abstract: Radio Frequency (RF) Integrated Circuits (ICs) are crucial circuits for modern wireless communication systems. Prompted by mobile applications such as GSM, 3G, WiFi, WiMAX and LTE, RFIC market is fast growing and very dynamic in the IC industry. However, these mobile applications bring challenges for the RFIC design with stringent and conflicting constraints of high performance, low power and low cost for mass adoption. There are three major trends for RFIC design to catering for different applications and progresses of the standards. Firstly, the operating frequency is moving towards higher frequency like 60GHz and beyond. Secondly, the operating bandwidth is becoming larger from MHz in GSM to several GHz in 60GHz radio. Thirdly, the power consumption is continually reducing prompted by portable applications. This talk presents recent progress on RFIC design for low-power 60GHz applications with consideration of these three major trends. It will also cover design issues from product definition to RF circuits, SOC design as well as co-design of SOC and packaging. Some innovative design techniques for VCO, switch, broadband AGC etc, used in 60GHz radio will be introduced.

Speaker Biography: Kaixue MA received the Ph.D degree from Nanyang Technological University (NTU), Singapore. From 1997 to 2002, he was with China Academy of Space Technology (Xi’an), where he was group leader of millimeter-wave group for space-borne microwave and millimeter-wave components and subsystems for satellite payload. From 2005 to 2007, he was with MEDs Technologies as an R&D Manager. From 2007 to 2010, he was with ST Electronics (Satcom & Sensor Systems) as R&D Manager and Technique Management Committee of ST Electronics. He developed Ka VSAT products selling in market for VSAT ground station. Since March 2010, he is with NTU as a Senior Research Fellow and RFIC team leader for 60GHz Flagship Chipset project SOC. As PI/technique leader, he successfully completed projects with fund more than S$12M (excluding projects done in China). He has applied 7 patents and 3 patents in pending in RF & millimeter-wave IC design and has authored or co-authored over 90 journal and conference papers. Dr Ma is a Senior Member of IEEE.
"A Novel 1TX/4RX 77GHz Radar System in 65nm CMOS with Digital Beamforming Technique"

Jri Lee
National Taiwan University, Taiwan

Abstract: This work presents a 77GHz automotive radar system including LTCC antenna and digital beamforming. Fully integrated in 65nm CMOS and assembled with flip-chip technique, the radar achieves 100m and +/- 8 degree detection distance and angle, respectively, in a tiny volume of 2.5cm x 4cm x 1cm.

Speaker Biography: Jri Lee is Professor of Electrical Engineering at National Taiwan University. His research includes wireless and wireline transceivers, high-speed communication systems, and mmwave techniques. He is serving or has served as SSCS Distinguished Lecturer, TPC members of ISSCC, VLSI Symposium, and A-SSCC. He received the Beatrice Winner Award at ISSCC2007 and Takuo Sugano at ISSCC2008.
"60GHz CMOS Transceiver Design for Mobile Applications Based on WiGig/IEEE802.11ad Standard"

Koji Takinami (Speaker), Noriaki Saito, Kazuaki Takahashi
Panasonic, Japan

Abstract: A 60GHz short range wireless system offers new opportunities for achieving wireless high-definition video links and multi-Gb/s wireless data transfer. Recent works have realized such a transceiver in a cost effective CMOS process, but using a 60GHz system in mobile terminals is extremely challenging to achieve low power consumption as well as small form factor. This talk addresses design challenge and recent progress of 60GHz transceiver developments targeting for mobile usage. The talk covers various design techniques such as a transformer-based compact LNA, a small quadrature hybrid, an auto calibrated PLL and etc. With those techniques, a 60GHz direct conversion transceiver is fabricated in a 90nm CMOS process. The developed transceiver achieves up to 1.76Gsps pi/2-BPSK/QPSK modulation with excellent distortion and spurious suppression that meet the IEEE802.11ad standard.

Short Biography: Koji Takinami received the B.S. and M.S. degrees in electrical engineering from Kyoto University, Kyoto, Japan, in 1995 and 1997, respectively. In 1997, he joined Matsushita Electric Industrial (Panasonic) Co., Ltd., Osaka, Japan. Since then he has been engaged in the design of analog and RF circuits for wireless communications. From 2004 to 2006, he was a visiting scholar at the University of California, Los Angeles (UCLA), where he was involved in the architecture and circuit design of the high efficiency CMOS power amplifier. In 2006, he joined Panasonic Silicon Valley Lab, Cupertino, CA, where he worked on high efficiency transmitters and low phase-noise digital PLLs. In 2010, he relocated to Japan and joined Communication Core Devices Development Center, Panasonic, where he currently leads the development of the millimeter wave transceiver ICs.